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DIGITAL SIGNAL PROCESSOR IN OPTICAL TOMOGRAPHY SYSTEM

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8.1 INTRODUCTION

Optical tomography involves the use of non-invasive optical sensors to obtain vital information in order to produce images of the dynamic internal characteristics of process system (Ibrahim et al., 2000). The use of optical sensors has the advantages of being conceptually straightforward and relatively inexpensive (Pang et al., 2004). Its working principle involves projecting a beam of light through a medium from one boundary point and detecting the level of light received at another boundary point (Rahim, 1996). A typical optical tomography system usually used DAQ to perform data acquisition tasks and host computer to carry out image reconstruction. However, only some of the functions provided by the DAQ were implemented. This is a waste

considering the high cost of a DAQ system. This paper discusses the implementation of DSP as the core processor in a parallel beam projection optical tomography system.

On the other hand, powerful Digital Signal Processor (DSP) running at Millions Instructions Per Second (MIPS) are getting available at very reasonable cost. DSP which is usually equipped with single cycle multiplication is well suited for number crunching applications and optimized for digital signal processing algorithms. The tasks that were carried out by the DAQ and host computer such as data acquisition and image reconstruction can now be carried out by the DSP alone. However, the host computer is still needed for display purpose. Alternatively, a Liquid Crystal Display (LCD) could be utilized to display the results.

8.2 HARDWARE CONSTRUCTION

8.2.1 Sensor Configuration

Two layers (Upstream and Downstream) of four parallel beam projections were implemented where each layer consisted of an orthogonal projection and a rectilinear projection. In each layer,

thirty two sensors were arranged in two orthogonal projections while forty six sensors were arranged in rectilinear projection to act as masking layer. For the two rectilinear projections, both arrays of projections are inclined plus minus 45º to the horizontal axis respectively. Such configuration reduces the detection of ambiguous image when the flowing materials are in certain arrangements (Pang et al., 2004). The sensor configuration

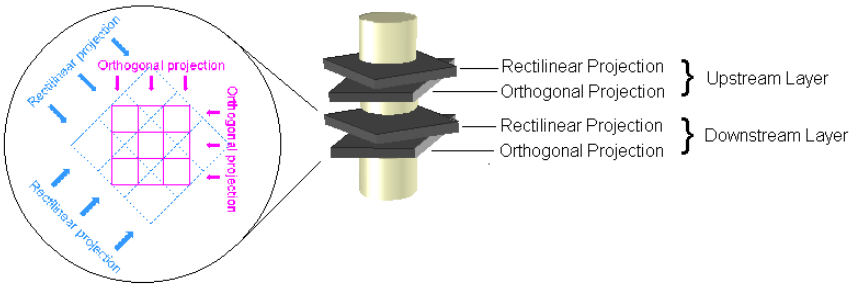

Figure 8.1 Sensor Configuration

8.2.2 Signal Conditioning

There were a total of 64 analogue sensor values (32 Upstream and 32 Downstream) that need to be converted to digital values in orthogonal projections. Eight dual 4-channel analogue

multiplexers (SN74LV4052A) were used to pass these values to the Analogue to Digital Converter (ADC) available internally in the chosen DSP. Each analogue multiplexer passed two analogue values at one time, thus resulting in sixteen analogue values arriving at the ADC input channels. Only four cycles were required to convert all the 64 channels. This configuration is shown in Figure 8.2.

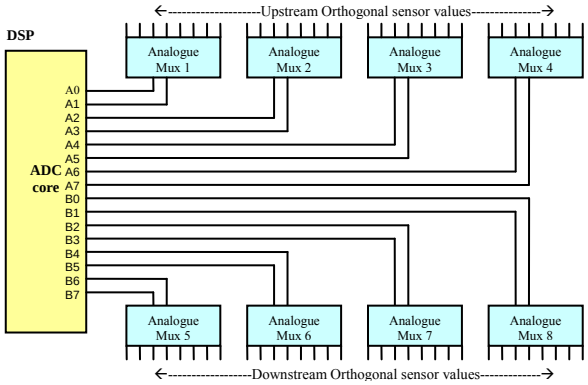

Figure 8.2 Analogue multiplexers configuration

On the other hand, 92 analogue sensor values from the rectilinear projections (46 Upstream and 46 Downstream) were compared to a threshold voltage to produce binary representation, i.e. a logic TRUE if the sensor voltage was higher than the

threshold voltage and a logic FALSE when the sensor voltage is lower than the threshold voltage. The threshold voltage was set to about a quarter of the full scale sensor voltage so that logic TRUE would be generated when more than a quarter of the sensor light beam was blocked. This was carried out using IC comparator where the reference voltage was the threshold voltage. The outputs of the comparator were fed to eight sets of parallel to serial converter (74HC165) wired in cascaded (serial out of previous set, Qo to serial in of the next set, Cin). This topology facilitated the use of Serial Peripheral Interface (SPI) to read the binary values. The SPI core was also available internally in the DSP.

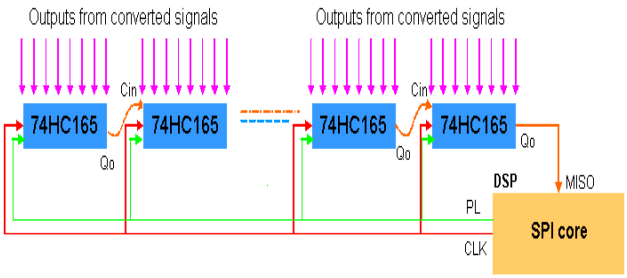

Figure 8.3 Serial Peripheral Interface (SPI) for digital sensor inputs

8.2.3 The Digital Signal Processor

The chosen DSP, TMS320 F2812 was manufactured by Texas Instruments Inc. It provides many useful features and is very powerful. Table 8.1 below summarizes the available features in the DSP

Table 8.1 DSP features

Feature	Description
Instruction Cycle (at 150 Mhz)	6.67 ns
Single Access RAM (16 bit word)	18 k
3.3 v on-chip Flash (16 bit word)	128 k
External Memory Interface	Available
General Purpose Timers	4
Analogue to Digital Converter (ADC)	12 bits, 16 channels, 80 ns conversion time
Serial Peripheral Interface (SPI)	Available
Serial Communication Interface (SCI)	Available, 2 channels
Digital I/O pins (shared)	56

8.3 FIRMWARE DEVELOPMENT

8.3.1 System Flowchart

The overall operation performed by the DSP is described in Figure 8.4 below.

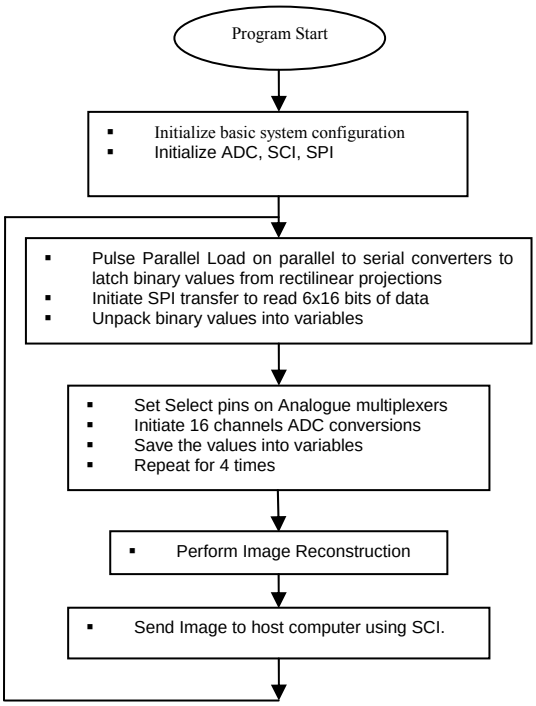

Figure 8.4 Overall System Flowchart

Basically, the system was initialized at program start to set the configurations of ADC, SPI and SCI such as ADC channel

sampling sequence, SCI and SPI bit length, parity and baud rate. After being initialized, data acquisition began by sending a pulse to Parallel Load pin on parallel to serial converters. This action latched the binary outputs from the comparator into the converter. Then, acquisition from rectilinear projection sensors was carried out by reading data from SPI. The use of SPI caused the binary values to be packed in six words, so they were unpacked into variables after the acquisition.

As for the orthogonal projections, the Select pins on the analogue multiplexers were set from 0 to 3 to multiplex 64 channels into the ADC. The Select pin setting and the respective channels being multiplexed are shown in Table 8.2 below.

Two image reconstruction algorithms were implemented in this study. The first algorithm was the commonly known Linear Back Projection algorithm while the second algorithm was the Hybrid algorithm (Ibrahim et al., 2002). The image reconstructed was stored in internal Random Access Memory (RAM) of the DSP. Finally, the DSP sent the image to the host computer upon request via SCI. At the host computer, a Graphical User Interface (GUI) was developed using Ms. Visual C++ to facilitate this feature.

Table 8.2 Analogue Multiplexers configuration

Select pins		**ADC channel**							
MSB	*LSB*	*A0*	*A1*	*A2*	*A3*	*A4*	*A5*	*A6*	*A7*
		B0	*B1*	*B2*	*B3*	*B4*	*B5*	*B6*	*B7*
		Orthogonal Sensor Array index							
0	0	0	1	2	3	4	5	6	7
0	1	8	9	10	11	12	13	14	15
1	0	16	17	18	19	20	21	22	23
1	1	24	25	26	27	28	29	30	31

8.3.2 DSP Optimization Techniques

Programming a DSP is not as straight forward as programming a high level programming language. Although the DSP could be programmed using a C compiler, the code implementation must be well considered in order to optimize for speed. Using a personal computer nowadays with Giga Hertz operating frequency almost have no noticeable delay but for a DSP running at only 150 MHz, some delay here and there could cause very noticeable system slow down. For instance, storing the image reconstructed in the DSP internal memory was faster than in the

external memory. This was because of the wait states required to acquire or put data to and fro the external interface. Besides that, calling functions with a lot of passing parameters also slows down the system considerably since the passed values need to be copied to the memory stack. On addition to that, passing parameters by reference or pointer is always faster than passing by value. The use of pointers prevents from copying the passed values which wastes time. Since this DSP is a fixed point processor, running floating point codes would slow down the system considerably too. This is due to the fact that floating point values usually requires 32 bit implementation. Thus, the DSP needed two cycles to fetch the data and some cycles to perform floating point to fixed point conversion routine.

8.4 RESULTS

The results acquired were evaluated in two categories. The first category was the execution speed while the second category was the quality of the reconstructed cross sectional image.

8.4.1 The Execution Speed

The execution speed can be measured easily by toggling a General Purpose Input Output (GPIO) pin and measuring the time delay using an oscilloscope. The timer function available in the DSP could was also used to measure the execution time. From experiments, the measured time using timer DSP is the same as using oscilloscope. A GPIO pin was set to HIGH at the beginning of data acquisition and set to LOW to represent the beginning of image reconstruction. Therefore, the overall time per frame was measured from a HIGH level to the next HIGH level. The time required per frame for one layer and both layers are shown in Table 8.3 below.

Table 8.3 Program Execution Time

Algorithm	One Layer	Both Layers
Linear Back Projection	233 us	313 us
Hybrid	305 us	466 us

The time required for data acquisition and processing is comparable to the time required in previous work by Pang (Pang et al., 2004) which needed 1.58 ms per frame. This improvement is mainly due to the use of high speed ADC core in the DSP, digital

sampling of rectilinear projection sensors and high speed execution using DSP.

8.4.2 The Reconstructed Image

Two small sticks (6 mm diameter), medium sized pipe (2.7cm diameter) and a large sized pipe (4.24 cm diameter) were used as samples to be imaged. The results are shown in Figure 8.5.

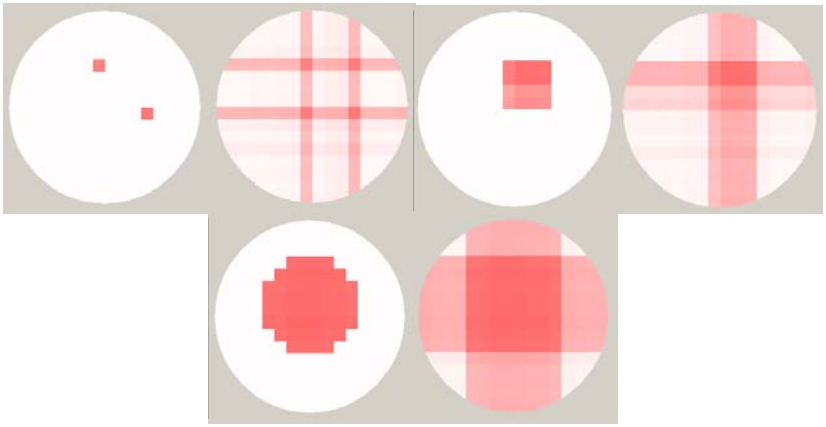

Figure 8.5 Reconstructed images

From Figure 8.5, each sample was shown with image reconstructed using Hybrid algorithm on the left and LBP algorithm on the right. The two pixels shown in the first image represents the two small sticks. The second image seems like four

pixels due to ambiguity. The fourth and the last image were also reconstructed using LBP and contains smearing. This smearing was eliminated using the Hybrid algorithm shown in first, third and fifth image.

8.5 CONCLUSION

The data acquisition and processing of a parallel beam projection optical tomography system was presented and discussed in this paper. The speed at which the DSP perform data acquisition and image reconstruction is comparable to previous work utilizing DAQ and host computer. This proves that DSP is a promising solution at a lower price, smaller board size and yet competitive in performance.

8.6 REFERENCES

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